1. A power-to-power semiconductor ESD protection structure on a semiconductor substrate comprising:

multiple first doped regions within said substrate of opposite dopant than said substrate;

a second doped region within each of said multiple first doped regions of opposite dopant type than said multiple first doped regions;

multiple third doped regions within said substrate of opposite dopant type from said substrate each of which together with one each of said second doped regions within one said first doped region forms a doped pair;

multiple conductor elements each one connecting one said third doped region of one said doped pair to one said second doped region of another said pair, starting with said third doped region of a first pair and ending with said second doped region of another pair, to form an electrical series string of said protection structure element pairs;

a conductor element from said second doped element of said first pair to a first voltage source; and

a conductor element from said third doped element of said n-th pair to a second voltage source.

2. The protection structure of claim 1 wherein said substrate is P doped with a concentration between 1E15 and 5E15 a/cm^3.

3. The protection structure of claim 1 wherein said multiple first doped regions are doped with a donor dopant to form N-well regions with a typical dopant density of between 1E16

and 1E18a/cm^3.

4. The protection structure of claim 1 wherein said second doped regions within each of said multiple first doped regions are doped with an acceptor dopant to form P+ regions with a dopant concentration between 1E20 and 1E21 a/cm^3.

5. The protection structure of claim 1 wherein said multiple third doped regions within said substrate are doped with a donor dopant to form multiple N+ regions with a dopant concentration of between 1E20 and 1E21 a/cm^3.

6. The protection structure of claim 1 wherein said second doped P+ region of said first doped pair is the anode of a first diode protection element and the emitter of a first parasitic bipolar PNP transistor.

7. The protection structure of claim 1 wherein said first doped N-well region is the cathode of said first diode protection element and also the base of said first parasitic bipolar PNP transistor and the collector of a first parasitic NPN bipolar transistor.

8. The protection structure of claim 1 wherein said substrate is the collector of said first PNP parasitic bipolar transistor, the base of said first parasitic NPN bipolar transistor, and the anode of a second diode protection element.

9. The protection structure of claim 1 wherein said third doped N+ region of said first doped pair is the cathode of said second diode protection element and the emitter of said first parasitic NPN bipolar transistor.

10. The protection structure of claim 1 wherein said second doped P+ region of said second doped pair is the anode of a third diode protection structure and the emitter of a

second parasitic PNP bipolar transistor.

11. The protection structure of claim 1 wherein said first doped N well region which contains said second doped P+ region of said second doped pair is the cathode of said third diode protection device structure and the base of said second parasitic PNP bipolar transistor.

12. The protection structure of claim 1 wherein said substrate is the collector of said second PNP parasitic bipolar transistor, the base of said second parasitic bipolar NPN transistor, and the anode of a fourth diode protection device structure.

13. The protection structure of claim 1 wherein said third doped N+ region of said second doped pair is the cathode of said fourth diode protection device, and the emitter of said second NPN parasitic transistor.

14. The protection structure of claim 1 wherein said protection structure element pairs are repeated for n dopant pairs, whereby n can assume the value from two to ten.

15. The protection structure of claim 1 wherein the first conductor element of said multiple conductor elements connects said third doped N+ region of said first doped pair to said second doped P+ region of said second doped pair and the n-1 conductor connects said third doped N+ region of the n-1 doped pair with said second doped P+ region of the n-th doped pair.

16. A power-to-power semiconductor ESD protection structure on a semiconductor substrate comprising:

a first doped region within said substrate of opposite dopant than said substrate;

a second doped region within said first doped region of opposite dopant type to said first doped region;

a third doped region within said substrate of opposite dopant type from said substrate which when taken with said second doped region within said first doped region forms a doped pair;

a conductor element from said second doped region to a first voltage source; and

a conductor element from said third doped region to a second voltage source.

17. The protection structure of claim 16 wherein said substrate is P doped with a concentration between 1E15 and 5E15 a/cm^3.

18. The protection structure of claim 16 wherein said first doped region is doped with a donor dopant to form a N-well region with a typical dopant density of between 1E16 and 1E18 a/cm^3.

19. The protection structure of claim 16 wherein said second doped region is doped with an acceptor dopant to form a P+ region within said N-well region to a concentration between 1E20 and 1E21 a/cm^3.

20. The protection structure of claim 16 wherein said third doped region within said substrate is doped with a donor dopant to form a N+ region with a concentration of 1E20 and 1E21 a/cm^3.

21. The protection structure of claim 16 wherein said second doped P+ region is the anode of a first diode protection structure and the emitter of a parasitic bipolar PNP transistor.

22. The protection structure of claim 16 wherein said first doped N-well region is the cathode of said first diode protection element and also the base of said parasitic bipolar PNP transistor and the collector of a parasitic NPN bipolar transistor.

23. The protection structure of claim 16 wherein said substrate is the collector of said PNP parasitic bipolar transistor, the base of said parasitic bipolar NPN transistor, and the anode of a second diode protection element.

24. The protection structure of claim 16 wherein said third doped region is the cathode of said second diode protection element and the emitter of said parasitic NPN bipolar transistor.

25. A method of forming a power-to-power semiconductor ESD protection structure on a semiconductor substrate comprising:

creating a first doped region upon said substrate of opposite dopent than said substrate;

creating a second doped region within said first doped region of opposite dopant than said first doped region;

creating a third doped region within said substrate outside of said first doped region of opposite dopant than said substrate;

creating a first conductor element from said second doped region to a first voltage source; and

creating a second conductor element from said third doped element to a second voltage source.

26. The method according to claim 25 whereby said first doped region is formed by ion implant using a donor dopant such as phosphorous with an ion implant energy of between 400 and 800 KeV and with a dopant concentration between 6E12 and 2E13 a/cm^2 to produce a N-well with a dopant density of between 1E16 and 1E18 a/cm^3.

27. The method according to claim 25 whereby said second doped region within said first doped region is formed by ion implant with an acceptor element such as boron with an ion implant energy of between 4 and 10 KeV and with a dopant concentration between 1E15 and 5E15 a/cm^2 to produce a P+ doped region with a dopant density of between 1E20 and 1E21 a/cm^3.

28. The method according to claim 25 whereby said third doped region is formed by ion implant with a donor element such as arsenic with an ion implant energy of between 20 and 80 KeV and with a dopant concentration between 1E15 and 6E15 a/cm^2 to produce a N+ doped region with a dopant density of between 1E20 and 1E21 a/cm^3.

29. The method according to claim 25 whereby a first diode ESD protection element anode is formed by said second doped region and the cathode is formed by said first doped region.

30. The method according to claim 25 whereby a parasitic bipolar PNP transistor emitter is formed by said second doped region, the base by said first doped region, and the collector is formed from said substrate.

31. The method according to claim 25 whereby a second diode ESD protection element anode is formed by said substrate and the cathode is formed by said third doped region.

32. The method according to claim 25 whereby a parasitic bipolar NPN collector is formed by said first doped region, the base by said substrate, and the emitter by said third doped region.

33. The method according to claim 25 whereby the first and second conductor element is formed from metallurgy such as aluminum, or aluminum doped with silicon.